REMARKS

Claims 1-4 and 7-12 are pending in this application. Claims 1-4 and 7 were examined on the merits in the last Office Action. Claims 8-12 remain withdrawn from consideration. With the present submission, claim 1 is amended, and claim 5 is canceled.

Claims 1-4 and 7 stand rejected under 35 U.S.C. § 103(a) as obvious over the prior art depicted in the present application, labeled "Admitted Prior Art (APA)," in view of **Cook et al.** (U.S. Patent No. 6,022,791) and **Chiang et al.** (U.S. Patent No. 5,817,572). Applicant respectfully traverses this rejection.

Base claim 1 describes a semiconductor device that includes both: (1) "a conductive wall ... in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof;" and (2) "a second insulation film that supports [a] conductive pattern laterally." The rejection relies on the APA as the primary reference upon which to base the obviousness rejection, but it is acknowledged in the Office Action (page 4) that the APA does not teach these identified claim features.

To justify the obviousness rejection, **Chiang et al.** is relied upon to suggest modifying the APA to have the claim features identified above. In particular, the Office Action states on page 5 that **Chang et al.** teach in Fig. 25 a conductive wall 393, 394 extending from a bottom principal surface of the interlayer insulation film 391 to a top principal surface thereof, and a second insulation film 323 (an etch stop layer) supporting the conductive pattern 360,361 laterally.

Applicant respectfully disagree with this interpretation of **Chang et al.** Elements 393 and 394 of **Chiang et al.** form a via plug, not a conductive *wall* extending continuously in the lateral direction. (See column 21, lines 5-10.) Therefore, the prior art as combined in the Office Action does not suggest a semiconductor device with all elements recited in the claims. Under MPEP § 2143, a *prima facie* case of obviousness has not been established (due to failure to satisfy the third criterion).

Further, **Chiang et al.**, in column 2, line 20 *et seq.*, teach away from the dual damascene process using Cu reciting various associated problems, including the difficulty of controlling the depth of etching. Thus, there is no motivation for a person skilled in the art to combine the features of **Chiang** with the APA.

Applicant acknowledges that **Chiang et al.** teach formation of a Cu pattern 361 in Figs. 23 and 24, but this formation is part of a *single* damascene process, not a dual damascene process in which a via hole and an interconnection groove are formed simultaneously by a single etching step. As noted above, the cited portion of **Chiang et al.** addresses the difficulty of controlling the depth when conducting such an etching process.

Accordingly, applicant amends base claim 1 as shown above to emphasis the distinction between the present invention and the applied prior art. Withdrawal of the obviousness rejection is now requested.

Applicant now submits that the entire application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is felt that this application is not now in condition for allowance, the Examiner is invited to contact applicant's undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version of Amendments with Markings to Show Changes Made**."

In the event that this paper is not timely filed, applicant respectfully petitions for an appropriate extension of time. The fees for such an extension, or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully Submitted,
ARMSTRONG, WESTERMAN & HATTORI, LLP

Joseph L. Felber
Attorney for Applicant
Reg. No. 48,109

JLF/llf

Atty. Docket No. **000294**
Suite 1000,1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosure: Version of amendments with markings to show changes made

Q:\FLOATERS\JLF\00\000294\PREL AMEND 1-30-03

VERSION OF AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Four Times Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate,

and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally,

said conductive wall and conductive pattern comprising Cu.